CLAIMS:

1. A clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;
wherein said clusters are fully-connected to each other; and
wherein the latency of the connections between said clusters is dependent on the distance between said clusters.

2. Processor according to claim 1, comprising at least one pipeline register arranged between each two clusters.

3. Processor according to claim 2, wherein the number of pipeline registers between two clusters depend on the distance between said two clusters.

4. Processor according to claim 1, wherein the clusters are connected to each other via a point-to-point connection.

5. Processor according to claim 1, wherein the clusters are connected to each other via a bus connection.

6. Processor according to claim 5, wherein
- said bus connection is adapted for connecting said clusters and comprises a plurality of bus segments, and
said processor further comprising:
- switching means, arranged between adjacent bus segments, for connecting or disconnecting adjacent bus segments.

7. Processor according to claim 6, wherein said bus connection is a multi-bus comprising at least two busses.